In th Claims

CLAIMS

1. (Original) A four terminal memory cell comprising:

a first switching device having a control terminal and first and second load terminals, a first of the load terminals being coupled to a row line;

a first load element having a first terminal coupled to the second load terminal and having a second terminal coupled to a column line;

a second switching device having a control terminal and first and second load terminals, the first load terminal of the second switching device being coupled to the control terminal of the first switching device, the second load terminal of the second switching device being coupled to a first power supply and the control terminal of the second switching device being coupled to the second load terminal of the first switching device; and

a second load element having a first terminal coupled to a second power supply and a second terminal coupled to the second load terminal of the second switching device.

2. (Original) The memory cell of claim 1, wherein the memory cell comprises an area of $8F^2$, or less, wherein F represents one-half of a minimum lithographic pitch of the memory cell.

3. (Original) The memory cell of claim 1, wherein the first switching device comprises a NMOS transistor with the control terminal corresponding to a gate of the NMOS transistor, the first load electrode corresponding to a source of the NMOS transistor.

4. (Original) The memory cell of claim 1, wherein the second switching device comprises a PMOS transistor.

5. (Original) The memory cell of claim 1, wherein the first switching device corresponds to an ultrathin MOSFET of a first polarity and wherein the second switching device corresponds to an ultrathin MOSFET of a second polarity different than the first polarity.

6. (Original) The memory cell of claim 1, wherein the control electrode of the first switching device is formed from the second load element and the control electrode of the second switching device is formed from the first load element.

7. (Original) The memory cell of claim 1, wherein the first switching device corresponds to an ultrathin MOSFET of a first polarity and wherein the second switching device corresponds to an ultrathin MOSFET of a second polarity different than the first polarity, and wherein the control electrode of the first switching device is formed from the second load element and the control electrode of the second switching device is formed from the first load element.

Claims 8-14 (Cancelled)

15. (Original) A SRAM array forming a memory comprising a first line having a first potential, a second line having a second potential, a plurality of row lines, a plurality of column lines and a plurality of memory cells, each memory cell of the plurality comprising:

a first switching device having a control terminal and first and second load terminals, a first of the load terminals being coupled to one of the plurality of row lines;

a first load element having a first terminal coupled to the second load terminal and having a second terminal coupled to one of the plurality of column lines; and

a second switching device having a control terminal and first and second load terminals, the first load terminal of the second switching device being coupled to the control terminal of the first switching device, the second load

terminal of the second switching device being coupled to the first line and the control terminal of the second switching device being coupled to the second load terminal of the first switching device; and

a second load element having a first terminal coupled to the second line and a second terminal coupled to the second load terminal of the second switching device.

16. (Original) The SRAM of claim 15, wherein:

the first switching device comprises a first ultrathin transistor; and

the second switching device comprises a second ultrathin transistor.

17. (Original) The SRAM of claim 15, wherein:

the first switching device comprises a NMOS transistor; and

the second switching device comprises a PMOS transistor.

18. (Original) The SRAM of claim 15, wherein the memory cell comprises an area of $8F^2$, or less, wherein F represents one-half of a minimum lithographic pitch of the SRAM.

19. (Original) The SRAM of claim 15, wherein:

the first switching device comprises a NMOS transistor wherein a gate of the NMOS transistor is merged with the second load element; and

the second switching device comprises a PMOS transistor wherein a gate of the PMOS transistor is merged with the first load element.

20. (Original) The SRAM of claim 15, wherein the first and second switching devices and the first and second load elements comprise polycrystalline material.

21. (Original) A SRAM cell having an area of $8F^2$, or less, wherein F represents one-half of a minimum lithographic pitch of the SRAM cell.

22. (Original) The SRAM cell of claim 21, wherein the SRAM cell forms a portion of a memory comprising a first line having a first potential, a second line having a second potential, a plurality of row lines, a plurality of column lines and a plurality of memory cells, each SRAM cell comprising:

a first switching device having a control terminal and first and second load terminals, a first of the load terminals being coupled to one of the plurality of row lines;

a first load element having a first terminal coupled to the second load terminal and having a second terminal coupled to one of the plurality of column lines; and

a second switching device having a control terminal and first and second load terminals, the first load terminal of the second switching device being coupled to the control terminal of the first switching device, the second load terminal of the second switching device being coupled to the first line and the control terminal of the second switching device being coupled to the second load terminal of the first switching device; and

a second load element having a first terminal coupled to the second line and a second terminal coupled to the second load terminal of the second switching device.

23. (Original) The SRAM cell of claim 21, further comprising:

a first load device;

a first ultrathin transistor having a power electrode coupled to the first load device;

a second load device; and

a second ultrathin transistor including a power electrode coupled to the second load device, wherein the first load device is merged with a control electrode of the second ultrathin transistor and vice versa.

24. (Original) The SRAM of claim 21, further comprising:

a first load device;

a NMOS transistor including a power electrode coupled to the first load device;

a second load device; and

a PMOS transistor including a power electrode coupled to the second load device, wherein a gate of the NMOS transistor is merged with the second load device and a gate of the PMOS transistor is merged with the first load device.

Claims 25-55 (Cancelled)

56. (New) The memory cell of claim 1, wherein the first and second switching devices and the first and second load elements are formed on a semiconductive substrate.

57. (New) The memory cell of claim 1, wherein the first and second switching devices and the first and second load elements are formed on a p-type monocrystalline silicon substrate.

58. (New) The memory cell of claim 1, further comprising:

a semiconductor substrate having a first conductivity type;

a diffusion region formed in the substrate and having a second conductivity type different than the first conductivity type;

a first dielectric pillar formed atop the diffusion region, the first switching device comprising a first FET, the first FET and the second load element being formed along one side of the first dielectric pillar; and

a second dielectric pillar formed atop the substrate, the second switching device comprising a second FET, the second FET and the first load element being formed along one side of the second dielectric pillar, the one side of each pillar facing the other pillar;.

59. (New) The memory cell of claim 58, wherein the first and second pillars have respective plan view areas of about F^2 and are separated by a distance of about F.

60. (New) The memory cell of claim 1, wherein the first and second switching devices comprise FETs and include polycrystalline silicon.

61. (New) The memory cell of claim 1, wherein the first and second load elements comprise polycrystalline material.

62. (New) The memory cell of claim 1, wherein the memory cell is configured to be turned OFF by increasing a voltage on the row line coupled to the second switching device above a threshold voltage for the second switching device.

63. (New) The memory cell of claim 1, wherein the memory cell is configured to be turned OFF by turning a row of memory cells OFF.

64. (New) The memory cell of claim 1, wherein the memory cell is configured to be turned OFF by raising a voltage coupled to the row line above a threshold voltage for the second switching device to turn a row of memory cells coupled to the row line OFF.

65. (New) The memory cell of claim 1, wherein the memory cell is configured to be turned OFF by turning OFF the first and second switching devices.

66. (New) The SRAM of claim 15, further comprising:

a semiconductor substrate having a first conductivity type, wherein each of the memory cells of the plurality further comprises:

a diffusion region formed in the substrate and having a second conductivity type different than the first conductivity type;

a first dielectric pillar formed atop the diffusion region, the first switching device comprising a first FET, the first FET and the second load element being formed along one side of the first dielectric pillar; and

a second dielectric pillar formed atop the substrate, the second switching device comprising a second FET, the second FET and the first load element being formed along one side of the second dielectric pillar, the one side of each pillar facing the other pillar,

67. (New) The SRAM of claim 66 wherein the first and second pillars have respective plan view areas of about F^2 and are separated by a distance of about F.

68. (New) The SRAM of claim 15, wherein each of the first and second switching devices comprise FETs and include polycrystalline silicon.

69. (New) The SRAM of claim 15, wherein each of the first and second load elements comprise polycrystalline material.

70. (New) The SRAM of claim 15, wherein each memory cell of the plurality is configured to be turned OFF by increasing a voltage on the one of the plurality of row lines coupled to the second switching device above a threshold voltage for the second switching device.

71. (New) The SRAM of claim 15, wherein the plurality of memory cells is organized into rows and columns, each row being coupled to a respective one of the plurality of row lines, and wherein each memory cell of the plurality is configured to be turned OFF by turning one row of memory cells coupled to one of the plurality of row lines OFF.

72. (New) The SRAM of claim 15, wherein the plurality of memory cells is organized into rows and columns, each row being coupled to a respective one of the plurality of row lines, and wherein each memory cell of the plurality is configured to be turned OFF by raising a voltage coupled to one of the plurality of row lines, corresponding to one row of memory cells, above a threshold voltage for the second switching device to turn the one row of memory cells OFF.

73. (New) The SRAM of claim 15, wherein each memory cell is configured to be turned OFF by turning OFF the first and second switching devices.

74. (New) The SRAM of claim 21, further comprising:

a semiconductor substrate having a first conductivity type;

a diffusion region formed in the substrate and having a second conductivity type different than the first conductivity type;

a first dielectric pillar formed atop the diffusion region;

a first FET of a first polarity type and including a gate, a source and a drain, the source being coupled to a first control line;

a first load element coupled between a second potential and the gate of the first FET;

a second FET of a second polarity type and including a gate, a source and a drain, the source of the second FET being coupled to the gate of the first

FET, the gate of the second FET being coupled to the drain of the first FET and the source of the second FET being coupled to a first potential;

a second load element having a first terminal coupled to the second line and a second terminal coupled to the second load terminal of the second switching device, the first FET and the second load element being formed along one side of the first dielectric pillar; and

a second dielectric pillar formed atop the substrate, the second FET and the first load element being formed along one side of the second dielectric pillar, the one side of each pillar facing the other pillar.

75. (New) The SRAM of claim 74 wherein the first and second pillars have respective plan view areas of about F^2 and are separated by a distance of about F.

76. (New) The SRAM of claim 21, wherein the SRAM cell forms a portion of a memory comprising a first line having a first potential, a second line having a second potential, a plurality of row lines, a plurality of column lines and a plurality of memory cells and wherein each memory cell of the plurality is configured to be turned OFF by increasing a voltage on the one of the plurality of row lines above a threshold voltage for a switching device included within each memory cell.

77. (New) The SRAM of claim 21, wherein the SRAM cell forms a portion of a memory comprising a first line having a first potential, a second line having a second potential, a plurality of row lines, a plurality of column lines and a plurality of memory cells, wherein the plurality of memory cells is organized into rows and columns, each row being coupled to a respective one of the plurality of row lines, and wherein each memory cell of the plurality is configured to be turned OFF by turning one row of memory cells coupled to one of the plurality of row lines OFF.

78. (New) The SRAM of claim 21, wherein the SRAM cell forms a portion of a memory comprising a first line having a first potential, a second line having a second potential, a plurality of row lines, a plurality of column lines and a plurality of memory cells, wherein the plurality of memory cells is organized into rows and columns, each row being coupled to a respective one of the plurality of row lines, and wherein each memory cell of the plurality is configured to be turned OFF by raising a voltage coupled to one of the plurality of row lines, corresponding to one row of memory cells, above a threshold voltage to turn the one row of memory cells OFF.

79. (New) The SRAM of claim 21, wherein the SRAM cell forms a portion of a memory comprising a first line having a first potential, a second line having a second potential, a plurality of row lines, a plurality of column lines and a plurality of memory cells each comprising first and second switching devices, wherein each memory cell is configured to be turned OFF by turning OFF the first and second switching devices.

80. (New) The SRAM of claim 22, further comprising first and second switching devices comprising FETs and including polycrystalline silicon.

81. (New) The SRAM of claim 22, wherein each of the first and second load elements comprise polycrystalline material.

82. (New) The memory cell of claim 1, wherein the memory cell comprises an area of $8F^2$, or less, wherein F is a minimum lithographic feature size.

83. (New) The SRAM of claim 15, wherein the memory cell comprises an area of $8F^2$, or less, wherein F is a minimum lithographic feature size.

84. (New) The SRAM of claim 21, wherein the cell is configured to utilize a plurality of electrons to store a single unit of information.

85. (New) The SRAM of claim 21, wherein the cell is configured to utilize at least one thousand electrons to store a single unit of information.

86. (New) The SRAM of claim 21, wherein the cell is configured to statically store a single unit of information.

87. (New) The SRAM of claim 21, wherein the cell is configured to utilize a plurality of electrons to statically store a single unit of information.

88. (New) A SRAM cell having an area of $8F^2$, or less, wherein F is a minimum lithographic feature size.

89. (New) A memory apparatus comprising:

a SRAM cell having an area of $8F^2$, or less, wherein F is a minimum lithographic feature size.